AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a dynamically adjustable threshold voltage associated with the silicon based semiconductor transistor device, and which dynamically adjustable threshold voltage is controlled at least in part using a bias voltage applied across the gate and source region of the semiconductor transistor device,

wherein said dynamically adjustable threshold voltage is caused by a trapping and detrapping mechanism associated with charge carriers in a channel region of the silicon based semiconductor transistor device.

Claim 2 (original): The silicon based semiconductor transistor device of claim 1, further wherein said gate and source region are located on a silicon on insulator substrate.

Claim 3 (cancelled)

Claim 4 (original): The silicon based semiconductor transistor device of claim 1, wherein said dynamically adjustable threshold voltage can be altered while the device is turned on.

Claim 5 (cancelled)

Claim 6 (cancelled)

Claim 7 (cancelled)

Claim 8 (original): A silicon based semiconductor field effect transistor (FET) which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region and comprising:

a channel conduction control region, which channel conduction control region is part of the FET gate and is adapted to generate a first electric field which controls a density of electrons available for conduction in the channel region of the FET;

wherein said first electric field operates to counter a movement of carriers into the channel region caused by a separate second electric field associated with a gate bias voltage applied to the FET;

and further wherein said threshold voltage can be dynamically adjusted during operation of the silicon based semiconductor device using said gate bias voltage.

Claim 9 (original): The FET of claim 8, wherein said first electric field generated by said channel conduction control region is controlled in part by said gate bias voltage.

Claim 10 (original): The FET of claim 8 wherein said first electric field generated by said channel conduction control region is controlled in part by a drain bias voltage.

Claim 11 (original): The FET of claim 8, wherein said channel conduction control region is doped with an impurity type which is the same as a substrate region of the FET, and opposite to an impurity type used in said source region and said drain region.

Claim 12 (original): A silicon based semiconductor field effect transistor (FET) which includes a gate, a source region

containing a first dopant of a first conductivity type, a drain region also containing said first conductivity type dopant, and a channel region coupling the source region and drain region, comprising:

a channel conduction control region, which channel conduction control region is part of the gate and contains a second dopant opposite said first conductivity type, said channel conduction control region being responsive to a gate bias voltage applied to the FET, and operating to generate a first electric field which controls a density of electrons available for conduction in the channel region of the FET;

wherein said first electric field operates to counter conduction in the channel caused by a separate electric field resulting from the gate bias voltage applied to the FET;

wherein a threshold voltage of the FET can be dynamically adjusted during operation of the silicon based semiconductor device using said gate bias voltage.

Claim 13 (original): The FET of claim 12, wherein said FET can be operated with a negative differential resistance mode.

Claim 14 (currently amended): In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a dynamically adjustable threshold voltage associated with the silicon based semiconductor transistor device, and which threshold voltage is adjusted at least in part under control of a bias voltage applied across the source region and drain region of the semiconductor transistor device,

wherein said semiconductor transistor device can be operated with a negative differential resistance mode.

Claim 15 (original): The silicon based semiconductor transistor device of claim 14, wherein said bias voltage can be used to turn off said device independently of a gate bias voltage.

Claim 16 (cancelled)

Claim 17 (original): In a silicon based semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, the improvement comprising:

a dynamically adjustable threshold voltage associated with the silicon based semiconductor transistor device, and which threshold voltage is adjusted using a first bias voltage applied across the source region and drain region of the silicon based semiconductor transistor device, and a second bias voltage applied across the source region and gate of the silicon based semiconductor transistor.

Claim 18 (original): The silicon based semiconductor transistor device of claim 17, wherein said device can be operated with a negative differential resistance (NDR) mode in response to a separate NDR bias signal applied to the device.

Claim 19 (original): The silicon based semiconductor transistor device of claim 17, wherein said device is formed as part of a memory circuit.

Claim 20 (original): The silicon based semiconductor transistor device of claim 17, wherein said dynamically adjustable threshold voltage can be adjusted up or down at approximately the same rate.

Claim 21 (new): A semiconductor device comprising:

a gate;

a source region;

a drain region;

a channel region coupling the source region and the drain region; and

a dielectric layer disposed between the gate and the channel region, the dielectric layer comprising a plurality of charge traps located in close proximity to an interface between the dielectric layer and the channel region,

wherein the channel region has a graded doping profile that provides a dopant concentration that peaks at a relatively small distance below the interface between the dielectric layer and the channel region.

Claim 22 (new): The semiconductor device of Claim 21, wherein the dopant concentration in the channel region peaks at less than 30 nm below the interface between the dielectric layer and the channel region.

Claim 23 (new): The semiconductor device of Claim 21, wherein the graded doping profile is sized to generate a vertical electric field in the channel region greater than 10^6 V/cm when the semiconductor device is turned on.

Claim 24 (new): The semiconductor device of Claim 21, wherein the plurality of charge traps are located within 1.5 nm of the interface between the dielectric layer and the channel region.

Claim 25 (new): The semiconductor device of Claim 21, wherein the drain region includes a lightly doped drain region at a junction between the channel region and the drain region.